AMENDMENTS TO THE CLAIMS

The following listing of claims will replace all previous listings of claims in the present application.

What is Claimed is:

1-8. (Canceled).

9. (Currently Amended) A semiconductor device comprising:

a board,

first and second intermediate substrates mounted on said board apart from each other, and

a first semiconductor chip having a first surface on which a plurality of first pads are formed and a second surface opposed to said first surface, said semiconductor chip being mounted over said first and second intermediate substrates in such a manner that a part of said second surface of said semiconductor chip faces said first intermediate substrate and another part of said second surface of said semiconductor chip faces said second intermediate substrate;

wherein said first intermediate substrate has a plurality of first bonding pads and said second intermediate substrate has a plurality of second bonding pads, each of said first bonding pads of said first intermediate substrate being electrically connected to an associated one of said first pads of said first semiconductor chip, and each of said second bonding pads being electrically connected to an associated one of said first pads of said first semiconductor chip.

10. **(Currently Amended)** A [[The]] semiconductor device ~~as claimed in claim 9,~~ comprising:

a board,

first and second intermediate substrates mounted on said board apart from each other, and

a first semiconductor chip having a first surface on which a plurality of first pads are formed and a second surface opposed to said first surface, said semiconductor chip being mounted over said first and second intermediate substrates in such a manner that a part of said second surface of said semiconductor chip faces said first intermediate substrate and another part of said second surface of said semiconductor chip faces said second intermediate substrate;

wherein said first intermediate substrate has a plurality of first bonding pads and said second intermediate substrate has a plurality of second bonding pads, each of said first bonding pads of said first intermediate substrate being connected via a first wire to an associated one of said first pads of said first semiconductor chip, and each of said second bonding pads being connected via a second wire to an associated one of said first pads of said first semiconductor chip.

11. **(Previously Presented)** The semiconductor device as claimed in claim 10, wherein said first intermediate substrate further has a plurality of third bonding pads each electrically connected to a corresponding one of said first bonding pads, and said second intermediate substrate further has a plurality of fourth bonding pads each electrically

connected to a corresponding one of said second bonding pads, each of said third and fourth bonding pads being led out externally via a conductive line.

12. **(Previously Presented)** The semiconductor device as claimed in claim 11, wherein said conductive line is connected to said board to form an electrical path between said board and each of said third and fourth bonding pads.

13. **(Currently Amended)** The semiconductor device as claimed in claim [[9]] 10, wherein each of said first and second intermediate substrates is formed in a rectangular shape, and either one side of the rectangular shape is less than 20 mm in length.

14. **(Currently Amended)** The semiconductor device as claimed in claim [[9]] 10, wherein said first and second intermediate substrates are formed of a silicon substrate.

15. **(Previously Presented)** The semiconductor device as claimed in claim 14, wherein said silicon substrate includes electronic components formed therein.

16. **(Currently Amended)** A [[The]] semiconductor device ~~as claimed in claim 15,~~ comprising:

a board,

first and second intermediate substrates mounted on said board apart from each other, and

a first semiconductor chip having a first surface on which a plurality of first pads are formed and a second surface opposed to said first surface, said semiconductor chip being mounted over said first and second intermediate substrates in such a manner that a part of said second surface of said semiconductor chip faces said first intermediate substrate and another part of said second surface of said semiconductor chip faces said second intermediate substrate;

wherein said first and second intermediate substrates ~~electronic components~~ include at least one of a capacitor and a resistor.

17. **(Previously Presented)** The semiconductor device as claimed in claim 9, further comprising a second semiconductor chip having a third surface on which a plurality of second pads are formed and a fourth surface which opposes said third surface, said second semiconductor chip being mounted over said first and second intermediate substrates in such a manner that a part of said fourth surface faces said first intermediate substrate and another part of said fourth surface faces said second intermediate substrate.

18. **(Currently Amended)** A [[The]] semiconductor device ~~as claimed in claim 17,~~ comprising:

a board,

first and second intermediate substrates mounted on said board apart from each other, and

a first semiconductor chip having a first surface on which a plurality of first pads are formed and a second surface opposed to said first surface, said semiconductor chip

being mounted over said first and second intermediate substrates in such a manner that a part of said second surface of said semiconductor chip faces said first intermediate substrate and another part of said second surface of said semiconductor chip faces said second intermediate substrate;

wherein said first intermediate substrate has a plurality of first bonding pads and a plurality of second bonding pads and said second intermediate substrate has a plurality of third bonding pads and a plurality of fourth bonding pads, each of said first bonding pads of said first intermediate substrate being connected via a first wire to an associated one of said first pads of said first semiconductor chip, each of said second bonding pads of said first intermediate substrate being connected via a second wire to an associated one of said second pads of said second semiconductor chip, each of said third bonding pads of said second intermediate substrate being connected via a third wire to an associated one of said first pads of said first semiconductor chip, and each of said fourth bonding pads of said second intermediate substrate being connected via a fourth wire to an associated one of said second pads of said second semiconductor chip.

19. (Previously Presented) The semiconductor device as claimed in claim 18, wherein said first intermediate substrate further has a plurality of fifth bonding pads each electrically connected to a corresponding one of said first and second bonding pads and said second intermediate substrate further has a plurality of sixth bonding pads each electrically connected to a corresponding one of third and fourth bonding pads, each of said fifth and sixth bonding pads being led out externally via a conductive line.

20. (Previously Presented) The semiconductor device as claimed in claim 19, wherein said conductive line is connected to said board to form an electrical path between said board and each of said first and second intermediate substrates.

21. (Previously Presented) The semiconductor device as claimed in claim 17, wherein each of said first and second intermediate substrates is formed in a rectangular shape and the length of either one side of the rectangular shape is less than 20 mm.

22. (Previously Presented) The semiconductor device as claimed in claim 17, wherein each of said first and second intermediate substrates is formed of a silicon substrate having electronic components formed therein, said electronic components including at least one of a capacitor and a resistor.

23. (New) A semiconductor device comprising:

a board;

first and second intermediate substrates mounted on said board apart from each other;

a first semiconductor chip having a first surface on which a plurality of first pads are formed and a second surface opposed to said first surface, said semiconductor chip being mounted over said first and second intermediate substrates in such a manner that a part oaf said second surface of said semiconductor chip faces said first intermediate substrate and another part of said second surface of said semiconductor chip faces said second intermediate substrate; and

a second semiconductor chip having a third surface on which a plurality of second pads are formed and a fourth surface which opposes said third surface, said second semiconductor chip being mounted over said first and second intermediate substrates in such a manner that a part of said fourth surface faces said first intermediate substrate without intervention of said first semiconductor chip and another part of said fourth surface faces said second intermediate substrate without intervention of said first semiconductor chip.